

Application No.: 09/990,995

Docket No.: JCLA7630

**REMARKS****Present Status of the Application**

The Office Action rejected all pending claims 1-12 and 14-15. Specifically, the Office Action rejected claims 6 and 8-15 under 35 U.S.C. 102(e), as being anticipated by Klinger (U.S. 6523071). The Office Action also rejected claims 1-5 and 7 under 35 U.S.C. 103(a) as being unpatentable over Klinger in view of common digital design techniques, as evidenced by Rackley (U.S. 5365122). Applicant states the reasons that the present application could be patented. Reconsideration of those claims is respectfully requested.

**Discussion of Office Action Rejections**

*Klinger does not disclose that the D flip-flop is reset by the system reset. Although Klinger states that "The value stored is then made available to the GPI/GPO device 36 via leads 44 as long as no new system reset occurs" (column 6, lines 59-61), Klinger does not state the D-latch is reset by the system reset. On the contrary, Klinger states that the D-latch (one example of the sampling circuit 41) having its own reset control (column 6, line 45) and the reset control signal is independent from the main reset signal (column 6, lines 32-34). Klinger does not suggest the reset control signal of the sampling circuit 41 (or D-latch) have any relationship to the system reset, further, the reset control signal is independent from the main reset signal, which is a signal obtained by delay the system reset.*

Application No.: 09/990,995

Docket No.: JCLA7630

Klinger does not deny the use of the system reset, however, *Klinger does not suggest the use of the system reset*, either. Cf. Kotzab, 217 F.3d at 1371 (“[P]articular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed.”). For further views on official notice, see *In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420-421 (CCPA 1970) (“[A]ssertions of technical facts in areas of esoteric technology must always be supported by citation of some reference work” and “allegations concerning specific ‘knowledge’ of the prior art, which might be peculiar to a particular art should also be supported.”

Accordingly, since Klinger *does not specify* to use the system reset as the reset control signal of the sampling circuit and Klinger *agrees different practical approaches may be used* for embodying this circuit (column 6, lines 43-44), the Examiner shall not assume that the system reset is the only choice to reset the sampling circuit (or D-latch).

Combining with Rackley, Rackley *dose not specify* that the signal R to the input terminal CLR is a system reset. Accordingly, since the selection to use the system reset did not specified by either Klinger nor Rackley, it is non-obvious for those with ordinary skill to choose the system reset as the D-latch reset signal for there being many other choices to do that.

Accordingly, claim 1 is patentable over Klinger in view of common digital design techniques, as evidenced by Rackley because combination of Klinger and Rackley does not disclose, teach or suggest the feature of “...wherein said clear terminal can be triggered by a system reset ...”.

Application No.: 09/990,995

Docket No.: JCLA7630

For at least the same reasons stated above, claims 2-5 are patentable over Klinger in view of common digital design techniques, as evidenced by Rackley as a matter of law since their depending claim is patentable.

For at least the same reasons stated above, claim 7 is patentable over Klinger in view of common digital design techniques, as evidenced by Rackley because combination of Klinger and Rackley does not disclose, teach or suggest the feature of "... wherein said latching device further includes a clear terminal such that said output terminal of said latching device is reset to a low potential when said clear terminal is triggered by a system reset signal ..." as claimed in claim 6, which is depended by claim 7.

The Office Action further rejected claims 6 and 8-15 under 35 U.S.C. 102(e), as being anticipated by Klinger. Applicant respectfully traverses the rejections for at least the reasons set forth below.

To anticipate a claim, the reference must teach each and every element of the claim. M.P.E.P. § 2131. However, according to the discussion set forth above, Klinger at least does not teach the feature of "...wherein said latching device further includes a clear terminal such that said output terminal of said latching device is reset to a low potential when *said clear terminal is triggered by a system reset signal*" as claimed in claim 6.

Therefore, Klinger differs from the present invention, as the D flip-flops 31 and 32 employed in the present invention are reset by the system reset signal. The present invention obviously provides a much-simplified circuit than that proposed by Klinger by claimed definition in claim 6 of the present application, and Klinger does not anticipate claim 6.

Application No.: 09/990,995

Docket No.: JCLA7630

For at least the same reasons, Klinger does not anticipate claims 7-12 and 14 as a matter of law.

For at least the same reasons, Klinger does not anticipate claim 15 since Klinger does not teach the feature of "... a plurality of latching devices connected to said IDE bus cable and said detection device; wherein each said latching device has a triggering terminal, a clear terminal and an output terminal ... *said clear terminal triggered by a system reset* so that said output terminal of said latching device is reset to a low potential ..." as claimed in claim 15.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 6 and 15 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2-5, 7-12 and 14 patently define over the prior art as well.

Application No.: 09/990,995

Docket No.: JCLA7630

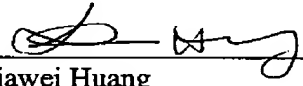
**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims 1-12 and 14-15 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date: 1/12/2005

4 Venture, Suite 250  
Irvine, CA 92618  
Tel.: (949) 660-0761  
Fax: (949)-660-0809

Respectfully submitted,  
J.C. PATENTS

  
Jiawei Huang  
Registration No. 43,330